5.7GHz 0.18μm CMOS Gain-Controlled LNA and Mixer For 802.11a WLAN Applications

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Abstract **—A 5.7 GHz 0.18μm CMOS gain-controlled differential LNA and a single-ended CMOS mixer for 802.11a WLAN applications are presented. The differential LNA, fabricated with the 0.18 μm 1P6M standard CMOS process, uses a current-reuse technology to increase linear gain and save power consumption. The single-ended CMOS mixer uses a single balance topology. Measurements of the CMOS components are performed by using a FR-4 PCB test fixture. The LNA exhibit noise figure of 3.7dB, linear gain of 12.5dB, P_{1dB} of –11dBm, and gain tuning range of 6.9dB. The mixer with a 280 MHz IF has a conversion gain -4.5dB, input P_{1dB} 0dBm, and noise figure 14.6dB. LO-RF isolation is 20dB and LO-IF isolation is 24dB. The power consumption of the differential LNA is 14.4mW and that of the mixer is 10.4mW from a 1.8V power supply.**

I. INTRODUCTION

Due to the fast growing demand for broadband wireless communications, the operating frequency is moving toward the 5 GHz U-NII band. The advantage of combining baseband and the RF front-end on one single chip for cost savings is strongly desired for highly integrated systems-on-chip (SOC) applications. Due to the speed improvements of the standard CMOS process, the unity gain frequency f_T of CMOS device becomes comparable to that in GaAs process. Recently, many RF circuits realized in the CMOS process have been reported and the 0.18 μm process is a good candidate for highly integrated SOC applications. The requirements of low power and low cost push the trend toward a single radio chip [1].. As shown in Fig.1, this paper presents a 5.7GHz gain-controlled differential CMOS LNA and a single balance mixer for 802.11a WLAN applications. They are fabricated in a TSMC 0.18-μm standard CMOS process. A current-reuse topology of a two-stage common source amplifier is adopted to share the operating current.[2] The fully differential LNA topology can mitigate the effects of common mode noise and clock feed-through. The function of controllable gain can prevent saturation of the receiver when the input signal is relatively large. The 5GHz CMOS single-ended mixer uses a single balance topology. The following section introduces circuit design flows of the differential LNA and mixer. .

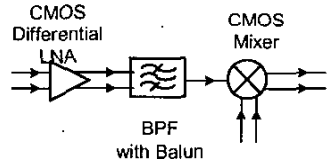

Fig.1 A 5.7 GHz CMOS gain-controlled differential LNA and CMOS mixer for 802.11a WLAN applications.

II. CMOS Gain Controlled Differential LNA

Fig. 2 illustrates the differential LNA with a current reuse topology. There are two virtual ground on the chip due to the chosen differential architecture. M_1 and M_2 transistors are both common source configurations, since the sources of M_1 and M_2 transistors are connected to signal ground separately. Two cascade common source amplifiers share the same supply current to reduce dc current consumption. Overall transconductance of the LNA topology is the multiplication of two cascade amplifier. It provides gain expansion. R_{bias1} and R_{bias2} are bias resistances. The bypass capacitance C_{bypass} achieves common source configuration of the second stage amplifier. L_{b1}~L_{b4} are bondwire equivalent inductances.

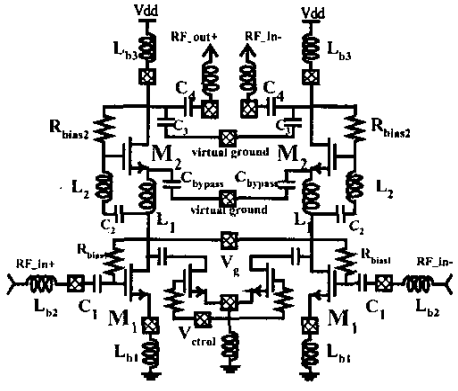

Fig. 2. Circuit schematic of a gain-controlled differential LNA with current reuse topology

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A. Input, Output and Inter-Stage Matching

From [6] the sources of noise and how to determine the gate width of the first stage transistor can be known. Under power consumption limit, the chosen gate width of the first stage transistor M_1 is 125(=25x5)μm. Multi-finger layout technology is used to reduce noise source of the transistor gate resistance. To achieve input matching to the 50Ω characteristic impedance of the system, we use series the bondwire equivalent inductance L_{b2}, the capacitance C_1 and the bondwire equivalent inductance L_{b1} of source-degeneration. The bondwire equivalent inductance L_{b1} is used to match the real part of the input impedance to the characteristic impedance. The combination of gate and source bondwire equivalent inductance cancels the reactance of the parasitic capacitance C_{gs} (at resonant frequency ω_o) of the input transistor M_1. The expressions of input impedance Z_{in} is shown as follow [3].

$$Z_{in} = s(L_{b1} + L_{b2}) + \frac{1}{sC_{gs}} + (\frac{g_{m1}}{C_{gs}})L_{b1} \qquad (1)$$

When at resonant frequency ω_o,

$$Z_{in} \approx \omega_T L_{b1} = 50\Omega \qquad (2)$$

where $\omega_T = g_{m1}/C_{gs}$, $\omega_o = 1/\sqrt{(L_{b1}+L_{b2})C_{gs}}$

The gate width of the second stage is chosen half width of the first stage. On chip inductance L_1 is used for the first stage inductive load so the resonant frequency of the chosen on chip inductor L_1 is closed to operating frequency range. Series on chip inductance L_2 and capacitance C_2 perform conjugated matching between the first and second stage. Using series capacitance C_4 and bondwire equivalent inductance L_{b4} perform output matching to the characteristic impedance of the system.

B. Gain -Controlled Mechanism

Fig. 3 illustrates the gain-controlled mechanism. The variable gain is controlled by the voltage applied to the switched transistor, which needs no extra dc current consumption.

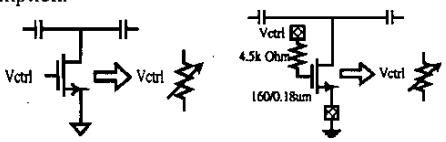


Fig. 3. Circuit schematic of gain-controlled switch transistor

C. Simulation and Measured Results

The LNA measurements are performed on a FR-4 PCB test fixture. As shown in Fig 4, the simulated/measured gain and input return loss are 14.5/12.5dB and 15.2/15dB, respectively, at 5.775GHz. Fig 5 shows the simulation and measurement of noise figure and controllable gain range, which are 3.65/3.7dB and 11.5/6.9dB, respectively. Fig. 6 shows the LNA layout and photograph of the FR-4 PCB test fixture. Table 1. summarizes the simulated and measured performance of the designed LNA.

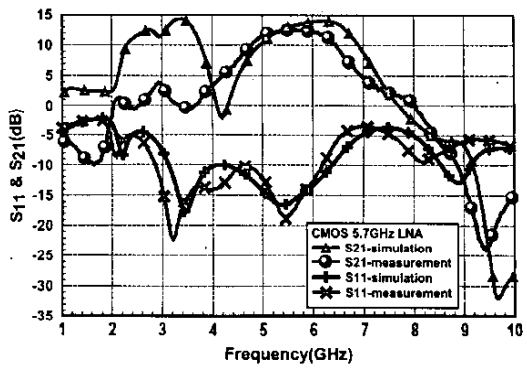


Fig. 4. Simulation and measurement results of the LNA gain and input return loss

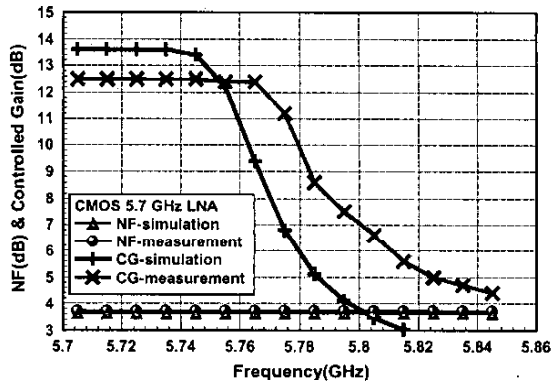


Fig. 5. Simulation and measurement results of the LNA noise figure and controlled gain range.

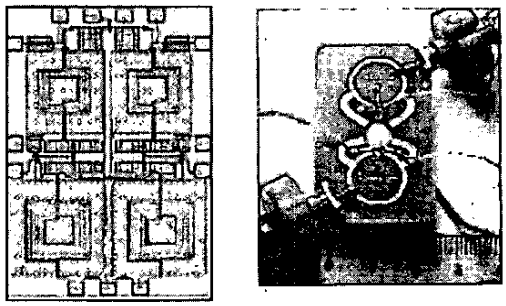


Fig. 6. Layout and photograph of the RF-4 PCB test board.(with two 180° microstrip hybrid ring couplers) of the designed LNA

Table 1 Simulated and measured performance of a 5.7 GHz 0.18-μm CMOS gain-controlled differential LNA.

5GHz 0.18μm Gain-Controlled Differential CMOS LNA		
	Simulation	Measurement
DC	1.8V/8mA	1.8V/8mA
Input / Output Return Loss	15.2/14dB	15/9dB
Gain	14.5dB	12.5 dB
Controlled Gain@0~1.8V	14.5dB~3dB	12.5dB~3.6dB
Input P_{1dB}	-13.5dBm	-11dBm
IIP3	-3.3dBm	-0.45dBm
Noise Figure	3.65dB	3.7dB
Die size	0.958x1.455mm^2	

III. CMOS SINGLE-ENDED MIXER

As shown in Fig.1, a single-ended mixer can be connected to the differential LNA through a differential-input/single-ended-output bandpass filter (BPF)-balun. Fig. 7 shows the architecture and operation principle of the singled-balanced mixer. The single-balanced mixer comprises an input trans-conductance stage and a differential switching stage. The trans-conductance amplifier M1 transfers the received RF signal into current format. Then, the switching pairs M_2 and M_3 (controlled by LO) perform the mixing operation, down-converting the RF signal into IF. Comparing with doubled-balanced mixer, the advantages of singled-balanced mixer include low noise figure, low power consumption and easy to design due to the simple circuitry. However, this architecture suffers from a poor LO-IF isolation performance. The IF circuits may need to handle high power LO leakage signal if the LO has not attenuated by IF filter sufficiently. Nevertheless, to the system that the LO frequency is much higher than IF like ours, the LO signal can be filtered out by IF filter easily. Therefore, it is not a very serious issue in our case.

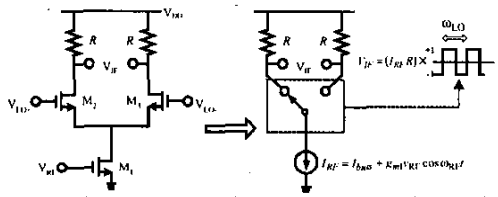


Fig. 7. Single-balanced mixer architecture and operation principle [4].

A. Circuit Design

Transcondutance, noise figure and linearity of the mixer are mostly governed by M_1. Considering the power consumption and the parameters mentioned earlier, the width of the M_1 was chosen to be 200μm. Transistors M_2 and M_3 are acting like a switching pair, the switching ability are the most important concern when deciding the width of the transistors. Larger transistor width implies that the loss of the switch could be lower. However, this will result in the situation of a higher parasitic capacitance of the transistor pair. The RF signal will be attenuated by these capacitors. Concerning the above design issues, the sizes of the M_2 and M_3 are chosen to be the same as the M_1.

The circuit schematic of the mixer is shown in Fig.8. The differential to single-ended output by using a passive balun is adopted [5] for higher linearity. Here a 2:1 balun (TOKO 616PT-1028) is added at the mixer output when in measurement. The insertion loss of the balun is 3dB. The RF and LO input matching use on-chip components and the IF output matching uses off-chip lumped components. The layout is shown in Fig. 9 with a chip size of 0.5 x 0.5 mm^2. Also shown in Fig. 9 (right) is the photography of the FR-4 PCB test fixture (with a off-chip balun) for measurement. Effects of bond-wires and the FR-4 test board were all taken into concern when performed simulation.

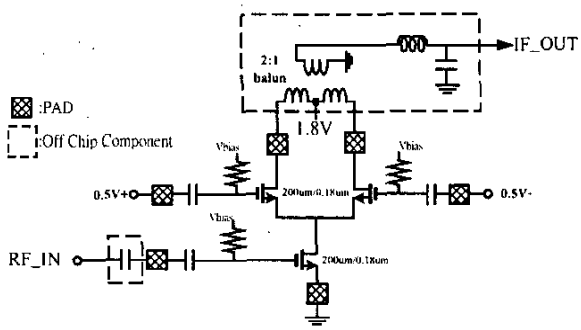


Fig. 8. Circuit schematic of a 5GHz CMOS single-balanced mixer.

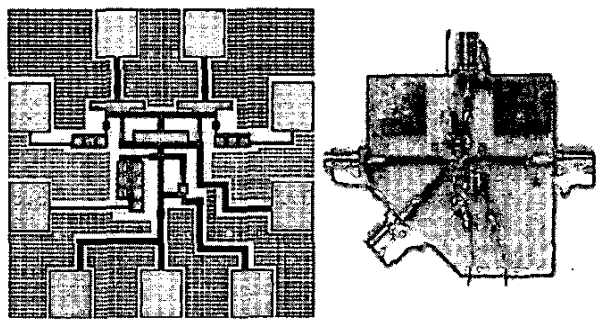
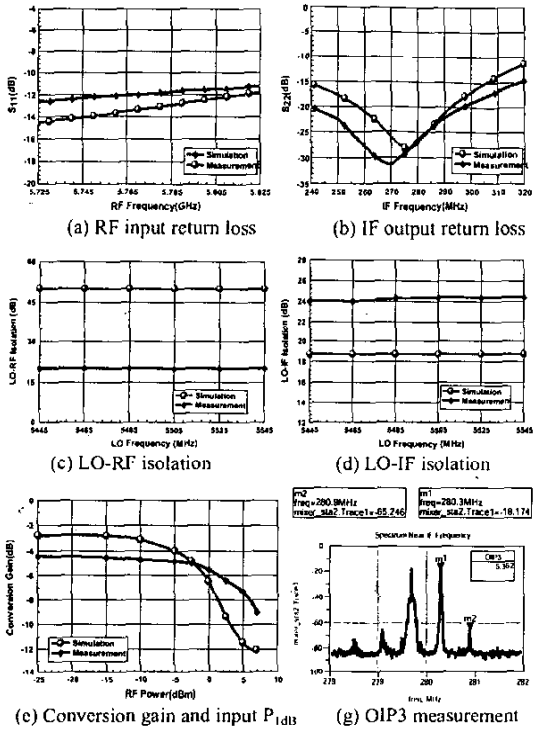


Fig.9. Layout and photograph of the RF-4 PCB test board of the 5GHz CMOS single-balanced mixer.

B. Simulation and Measurement

Using a 180° hybrid power divider connected to a RF signal generator provides the differential LO for measurement.. The mixer dissipates 10.8mW from a 1.8V supply. With RF from 5.725 to 5.825GHz and IF at 280MHz, the measured conversion loss is 4.5dB, input P_{1dB} is 0dBm, OIP3is 5.36dBm, noise figure is 14.6dB, LO-RF isolation is 20dB and LO-IF isolation is 24dB. The simulated and measured results of input/output matching, isolations, and conversion gain are shown in Fig. 10. Table 2. summarizes the simulated and measured performance of the mixer.



(a) RF input return loss (b) IF output return loss

(c) LO-RF isolation (d) LO-IF isolation

(e) Conversion gain and input P_{1dB} (g) OIP3 measurement

Fig. 10. Simulation and measurement results of the 5GHz CMOS single-balanced mixer.

IV. CONCLUSION

5.7 GHz CMOS components of a gain-controlled differential LNA and a single-ended CMOS mixer by using the 0.18μm technology for 802.11a WLAN applications are presented. The CMOS differential LNA uses current-reuse technology to increase linear gain and save power consumption. The differential LNA measurement at 5.775GHz exhibits noise figure of 3.7dB, linear gain of 12.5dB, P_{1dB} of −11dBm, and gain tuning range of 6.9dB with a power consumption of 14.4mW at 1.8V. For the single-balanced mixer, the differential to single-ended output by using a passive balun is adopted for higher linearity. A 2:1 balun is added at the mixer output when in measurement. The measured conversion gain is -4.5dB, input P_{1dB} is 0dBm and noise figure is 14.6dB, LO-RF isolation is 20dB and LO-IF isolation is 24dB. The power consumption of the mixer is 10.8mW at 1.8V. Further integration of the LNA and mixer in 0.18μm process will be pursued.

Table 2 Simulated and measured performance of a 5 GHz 0.18-μm CMOS mixer.

5GHz 0.18μm CMOS Single-Balanced Mixer		
RF Frequency	5.725~5.825GHz	
IF Frequency	280MHz	
LO Frequency	5.465~5.525GHz	
V_{dd}	1.8V	
	Simulation	Measurement
LO Power	0.5 V (amplitude)	4.5dBm
DC Current	6.2mA	6mA
Conversion Gain	-2.75dB	-4.5dB
Input Return Loss	13dB@5.8GHz	11.5dB@5.8GHz
Output Return Loss	29dB@280MHz	26.7dB@280MHz
LO-RF Isolation (LO=4.5dBm)	50dB	20dB
LO-IF Isolation (LO=4.5dBm)	18.7dB	24dB
Noise Figure	11.8dB	14.6dB
OIP_3	5.1dBm @RF=-20dBm	5.36dBm @RF=-15dBm
Input/Output P_{1dB}	-3.8dBm/-6.55dBm	0dBm/-4.5dBm

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